REMARKS

No amendments have been made. New claims 21-25 have been added. No new subject matter was added. Claims 1-25 remain pending. Reconsideration of claims 1-25 is respectfully requested in light of the following remarks.

Premature Final Rejection

Page 1 (status section) of the Office action mailed on November 14, 2002 (second Office action) indicates a non-final action. Nevertheless, the Examiner indicated that the applicant's amendments necessitated the new ground(s) of rejection presented in the second Office action and subsequently made that Office action FINAL (page 2, section 4).

To the contrary, the applicant wishes to point out that amendments to the claims were NOT made in response to the Office action mailed on July 22, 2002 (first Office action). Amendments to the specification were made in response to the first Office action, but only to correct typographical errors. Furthermore, the grounds of rejection presented by the Examiner in the second Office action (page 2, section 3) are the same as the grounds of rejection presented in the first Office Action (page 2, section 3). Thus, the current grounds of rejection are not new and were not necessitated by any amendment to the claims made by the applicant.

Additionally, the Examiner did not respond to the arguments made in reply to the grounds of rejection presented in the first Office action. With only a restatement of the previous grounds of rejection given in the present Office action, the applicant is unable to develop a clear issue between the applicant and Examiner, since it is unknown whether amendments to the claims are necessary or whether applicant's previous arguments are sufficient to overcome the Examiner's rejections. According to MPEP 706.07, where a single previous Office action contains a complete statement of the grounds of rejection, the final rejection may refer to such a statement and also should include a rebuttal of any arguments raised in the applicant's reply.

For these reasons, the applicant submits that the final rejection is premature and respectfully requests that the Examiner withdraw the finality of the second Office Action.

Claim Rejections – 35 USC § 103

Claims 1-20 were rejected under 35 USC §103(a) as unpatentable over applicant's prior art FIG. 1 in view of US Patent No. 5,994,732 issued to Ajika et al. ('Ajika'). The

Examiner states that it would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time the invention was made to modify Applicant's FIG. 1 Prior Art by the teaching as taught in Figs. 1-3 of Ajika et al., "*for the purpose of preventing well disturbance during the erase operation*" (emphasis added).

As explained above, because the grounds of rejection in the second Office action are the same as those presented in the first Office action, the applicant wishes to re-emphasize and resubmit the arguments made in the response to the first Office action. For the Examiner's convenience, these arguments are reproduced below:

> Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's FIG. 1 Prior Art in view of Ajika et al. (U.S. Patent No. 5,994,732). The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to form memory cell transistors of each sector on a common bulk region as taught by Ajika et al., "for the purpose of preventing well disturbance in the erase operation."
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> Applicant respectfully traverses the Examiner's rejection. There is no teaching or motivation to combine Ajika et al. with Applicant's FIG. 1 prior art. One of ordinary skill in the art would not have combined Ajika et al. with Applicant's FIG. 1 prior art for the reasons stated by the Examiner. In particular, Ajika et al. teaches away from larger bulk regions in order to reduce the effects of erase operations in one erase block on adjacent erase blocks. *See, e.g.*, FIGS. 9 and 4; col. 2, line 62-col. 3, line 28. In particular, Ajika et al. explains that "[s]ome erase blocks 26 may be falsely erased when a large number of erase blocks are arranged within the same p well region 3*a*." Col. 3, lines 22-24.
>
> Rather than extend the size and contents of the bulk region (e.g., p well), Ajika et al. teaches limiting the size and content of the p well *for the purpose of preventing well disturbance in the erase operation*. According to Ajika et al., "erase block 26 is preferably defined to include all of a plurality of memory transistors sharing one word line in one erase block 26. By limiting the size of an erase block to a single word line, the disturbance by the word line in the non-selected erase block can be effectively inhibited in the erase operation." Col. 7, line 65 – col. 8, line 2. The erase blocks are isolated from each other by forming an independent well for each erase block, "so that the well disturbance in the erase operation can be inhibited in a non-selected erase block." Col. 8, lines 7-11.
>
> Applicant's invention, on the contrary, teaches enlargement of the bulk well. Applicant's invention is not directed toward preventing well disturbance in the erase operation.

Furthermore, as can be seen in FIG. 4, the erase block of Applicant's invention includes more than a single word line. There is accordingly no motivation or teaching to combine Ajika et al. with Applicant's FIG. 1 prior art.

Not only is there no suggestion or motivation to combine, but the combination of Ajika FIG. 1-3 and applicant's prior art FIG. 1 does not cover all the claim limitations. This can be seen in the following discussion comparing Ajika FIGS. 1-3 to applicant's FIGS. 3-4.

It is first necessary to develop a grasp of exactly what is meant when Ajika refers to an "erase block." According to Ajika, "the word lines [10] extend parallel to a longitudinal direction of erase block 26" (column 7, lines 62-63). The erase block includes "all of a plurality of memory transistors sharing one word line in one erase block 26" (column 7, lines 65-67). The closest corresponding structure is shown by applicant's FIG. 3, where block 101 shows a plurality of word lines (WL0, WL1, WLn-1, etc) that are each shared by a plurality of memory transistors. Thus, Ajika's "erase block" corresponds to the memory transistors in applicant's FIG. 3 that share a single word line. Each "erase block" in applicant's FIG. 3 shares the same p-well, while it is apparent from Ajika FIG. 1 that each erase block 26 has an independent p-well region 3. Akija teaches that a principle of operation for his invention is forming an independent well for each erase block (column 8, line 7-11).

It might be argued that the entire memory cell array shown in applicant's FIG. 3 is equivalent to Ajika's "erase block", but this is not a valid argument because Ajika himself teaches away from such a suggestion. According to Ajika, a plurality of p-well regions exist in a memory cell array region of a flash memory, and each p-well region is electrically isolated from one another (FIG. 1; column 5, lines 66-67; column 6, lines 1-6; column 6, lines 38-41). There are two select gate transistors 12 provided at either end of every p-well region (column 6, lines 52-58). Between the two select gate transistors 12, there are a plurality of memory transistors 11 that form one erase block (column 6, lines 56-61).

New Claims 21-25

Five new claims are submitted for consideration. The new claims 21-25 are modeled after original independent claims 1, 5, 10, 15, and 18. The new claims distinguish from the combination of Ajika FIGS. 1-3 and applicant's prior art FIG. 1, as will be explained to the Examiner's satisfaction below.

New claims 21-25 emphasize that applicant is not claiming merely an "erase block" as defined by Ajika but a (M x N) array of memory cell transistors having at least two word

lines, where the common bulk region is shared among all transistors in the array, even by the transistors on different word lines. Even if Ajika's "erase block" could be considered a (M x N) array, despite Ajika's teaching away from such a consideration, the applicant now also claims column decoder transistors in a (1 x N) array as well. These new claims are supported by the original application in FIGS 3 and 4, and the new claim limitations are not suggested by Ajika.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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ON 6-9-03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 21-25 are new.